CLAIMS

We claim:

1. An integrated circuit layout, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

a third interconnect line layer, said third interconnect line layer having a first diagonal preferred direction of interconnect lines;

wherein said plurality of interconnect lines couple said plurality of circuit modules and at least one pair of parallel interconnect lines on one of said interconnect line layers are closer than line-to-via spacing using gridless routing.

2. The integrated circuit layout as claimed in claim 1, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction of interconnect lines, said second diagonal preferred direction orthogonal to said first diagonal preferred direction.

3. The integrated circuit layout as claimed in claim 2 wherein said first diagonal preferred direction is approximately forty-five degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative forty-five degrees relative to said preferred horizontal direction.

4. The integrated circuit layout as claimed in claim 1, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a preferred horizontal direction of interconnect lines.

5. The integrated circuit layout as claimed in claim 4, said integrated circuit layout further comprising:

a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction of interconnect lines, said second diagonal preferred direction orthogonal to said first diagonal preferred direction.

6. The integrated circuit layout as claimed in claim 1, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction of interconnect lines;

wherein said first diagonal preferred direction is approximately sixty degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative sixty degrees relative to said preferred horizontal direction.

7. The integrated circuit layout as claimed in claim 1, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction of interconnect lines;

wherein said first diagonal preferred direction is approximately negative sixty degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately positive thirty degrees relative to said preferred horizontal direction.

8. The integrated circuit layout as claimed in claim 1 wherein said integrated circuit layout is formed by compacting a gridded integrated circuit layout.

9. The integrated circuit layout as claimed in claim 1 wherein said pair of parallel interconnect lines may be placed as close together as can be manufactured reliably.

10. The integrated circuit layout as claimed in claim 1 wherein vias couple interconnect lines on different interconnect line layers.

11. A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first diagonal preferred direction of interconnect lines;

wherein said plurality of interconnect lines couple said plurality of circuit modules and at least one pair of parallel interconnect lines on one of said interconnect line layers are closer than line-to-via spacing using gridless routing.

12. The method of laying out said integrated circuit layout as claimed in claim 11, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction of interconnect lines, said second diagonal preferred direction orthogonal to said first diagonal preferred direction.

13. The method of laying out said integrated circuit layout as claimed in claim 11, said method wherein said first diagonal preferred direction is approximately forty-five degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative forty-five degrees relative to said preferred horizontal direction.

14. The method of laying out said integrated circuit layout as claimed in claim 11, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a preferred horizontal direction of interconnect lines.

15. The method of laying out said integrated circuit layout as claimed in claim 14, said method further comprising:

routing a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction of interconnect lines, said second diagonal preferred direction orthogonal to said first diagonal preferred direction.

16. The method of laying out said integrated circuit layout as claimed in claim 11, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction of interconnect lines;

wherein said first diagonal preferred direction is approximately sixty degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative sixty degrees relative to said preferred horizontal direction.

17. The method of laying out said integrated circuit layout as claimed in claim 11, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction of interconnect lines;

wherein said first diagonal preferred direction is approximately negative sixty degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately positive thirty degrees relative to said preferred horizontal direction.

18. The method of laying out said integrated circuit layout as claimed in claim 11 wherein said integrated circuit layout is formed by compacting a gridded integrated circuit layout.

19. The method of laying out said integrated circuit layout as claimed in claim 11 wherein said pair of parallel interconnect lines may be placed as close together as can be manufactured reliably.

20. The method of laying out said integrated circuit layout as claimed in claim 11 wherein vias couple interconnect lines on different interconnect line layers.

21. An integrated circuit, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect wiring layer, said first interconnect wiring layer having a plurality of parallel interconnect wires in horizontal direction;

a second interconnect wiring layer, said second interconnect wiring layer having a plurality of parallel interconnect wires in vertical direction; and

a third interconnect wiring layer, said third interconnect wiring layer having a plurality of parallel interconnect wires in a first diagonal direction;

wherein said plurality of interconnect wires couple said plurality of circuit modules and at least one pair of parallel interconnect wires on one of said interconnect wiring layers are closer than line-to-via spacing.

22. The integrated circuit as claimed in claim 21, said integrated circuit further comprising:

a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction, said second diagonal direction orthogonal to said first diagonal direction.

23. The integrated circuit as claimed in claim 22 wherein said first diagonal direction is approximately forty-five degrees relative to said horizontal direction and said second diagonal direction is approximately negative forty-five degrees relative to said horizontal direction.

24. The integrated circuit as claimed in claim 21, said integrated circuit further comprising:

a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a horizontal direction.

25. The integrated circuit as claimed in claim 24, said integrated circuit further comprising:

a fifth interconnect wiring layer, said fifth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction, said second diagonal direction orthogonal to said first diagonal direction.

26. The integrated circuit as claimed in claim 21, said integrated circuit further comprising:

a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction;

wherein said first diagonal direction is approximately sixty degrees relative to said horizontal direction and said second diagonal direction is approximately negative sixty degrees relative to said horizontal direction.

27. The integrated circuit as claimed in claim 21, said integrated circuit further comprising:

a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction;

wherein said first diagonal direction is approximately negative sixty degrees relative to said horizontal direction and said second diagonal direction is approximately positive thirty degrees relative to said horizontal direction.

28. The integrated circuit as claimed in claim 21 wherein said integrated circuit is formed from a compacted integrated circuit layout created by compacting a gridded integrated circuit layout.

29. The integrated circuit as claimed in claim 21 wherein said parallel interconnect wires may be placed as close together as can be manufactured reliably.

30. The integrated circuit as claimed in claim 21 wherein vias couple interconnect wires on different interconnect wiring layers.

31. A method of constructing an integrated circuit, said method comprising:

creating a plurality of circuit modules;

creating a first interconnect wiring layer, said first interconnect wiring layer having a plurality of parallel interconnect wires in a horizontal direction;

creating a second interconnect wiring layer, said second interconnect wiring layer having a plurality of parallel interconnect wires in a vertical direction; and

creating a third interconnect wiring layer, said third interconnect wiring layer having a plurality of parallel interconnect wires in a first diagonal direction;

wherein said plurality of interconnect wires couple said plurality of circuit modules and at least one pair of parallel interconnect wires on one of said interconnect wiring layers are closer than line-to-via spacing.

32. The method of constructing said integrated circuit as claimed in claim 31, said method further comprising:

creating a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction, said second diagonal direction orthogonal to said first diagonal direction.

33. The method of constructing said integrated circuit as claimed in claim 31, said method wherein said first diagonal direction is approximately forty-five degrees relative to said horizontal direction and said second diagonal direction is approximately negative forty-five degrees relative to said horizontal direction.

34. The method of constructing said integrated circuit as claimed in claim 31, said method further comprising:

creating a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a horizontal direction.

35. The method of constructing said integrated circuit as claimed in claim 34, said method further comprising:

creating a fifth interconnect wiring layer, said fifth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction, said second diagonal direction orthogonal to said first diagonal direction.

36. The method of constructing said integrated circuit as claimed in claim 31, said method further comprising:

creating a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction;

wherein said first diagonal direction is approximately sixty degrees relative to said horizontal direction and said second diagonal direction is approximately negative sixty degrees relative to said horizontal direction.

37. The method of constructing said integrated circuit as claimed in claim 31, said method further comprising:

creating a fourth interconnect wiring layer, said fourth interconnect wiring layer having a plurality of parallel interconnect wires in a second diagonal direction; wherein said first diagonal direction is approximately negative sixty degrees relative to said horizontal direction and said second diagonal direction is approximately positive thirty degrees relative to said horizontal direction.

38. The method of constructing integrated circuit as claimed in claim 31 wherein said integrated circuit is manufactured from a compacted integrated circuit layout created by compacting a gridded integrated circuit layout.

39. The method of constructing said integrated circuit as claimed in claim 31 wherein parallel interconnect wires on specific interconnect wiring layer may be placed as close together as can be manufactured reliably.

40. The method of constructing said integrated circuit as claimed in claim 31 wherein vias couple interconnect wires on different interconnect wiring layers.

41. A method of creating a compacted non Manhattan integrated circuit layout, said method comprising:

creating a group of horizontal interconnect lines and diagonal interconnect lines sorted by relative vertical position;

vertically compacting said group of horizontal interconnect lines and diagonal interconnect lines sorted by relative vertical position;

creating a group of vertical interconnect lines and diagonal interconnect lines sorted by relative horizontal position; and

horizontally compacting said group of vertical interconnect lines and diagonal interconnect lines sorted by relative horizontal position.

42. The method of claim 41 wherein creating said group of horizontal interconnect lines and diagonal interconnect lines sorted by relative vertical position comprises creating more than one subgroups of horizontal or diagonal interconnect lines that are independent.

43. The method of claim 42 wherein a vertical interconnect line in a first subgroup may be related to a diagonal interconnect line in a second subgroup.

44. The method of claim 41 wherein creating said group of vertical interconnect lines and diagonal interconnect lines sorted by relative horizontal position comprises creating more than one subgroups of vertical interconnect lines or diagonal interconnect lines that are independent.

45. The method of claim 44 wherein a horizontal interconnect line in a first subgroup may be related to a diagonal interconnect line in a second subgroup.

46. The method of claim 41 wherein said diagonal interconnect lines comprise 45° angle interconnect lines.

47. The method of claim 41 wherein said diagonal interconnect lines comprise minus 45° angle interconnect lines.

48. The method of claim 41 wherein creating a group of horizontal and diagonal interconnect lines sorted by relative vertical position comprises creating a graph of horizontal and diagonal interconnect lines arranged by relative vertical position.

49. The method of claim 41 wherein said diagonal interconnect lines comprise 60° angle interconnect lines.

50. The method of claim 41 wherein said steps of compacting comprise routing interconnect lines around obstacles.

51. A method of laying out an integrated circuit, said method comprising:

routing a first layer with a horizontal layer using a first defined wiring pitch;

routing a second layer with a vertical layer using said first defined wiring pitch;

routing a third layer with a first diagonal layer using said second defined wiring pitch;

routing a fourth layer with a second diagonal layer using said second defined wiring pitch; and

creating a first via at a first location where interconnect lines from at least three layers intersect.

52. The method of claim 51 wherein said first diagonal layer comprises interconnect lines at approximately 45 degrees.

53. The method of claim 531 wherein said first fist defined wiring pitch equals said second defined wiring pitch.

54. The method of claim 51 further comprising:

creating a second via at a second location where interconnect lines from at least two layers intersect and adding a zag to couple an interconnect line from a third layer to said second via.

55. A method of laying out an integrated circuit, said method comprising:

routing a first layer with a horizontal layer using a first defined wiring pitch;

routing a second layer with a vertical layer using said first defined wiring pitch;

routing a third layer with a first diagonal layer using said second defined wiring pitch;

routing a fourth layer with a second diagonal layer using said second defined wiring pitch; and

creating a first via at a first location where interconnect lines from two layers intersect and adding a zag to couple an interconnect line from a third layer to said second via.

56. The method of claim 55 wherein said first diagonal layer comprises interconnect lines at approximately 45 degrees.

57. The method of claim 55 wherein said first fist defined wiring pitch equals said second defined wiring pitch.

58. The method of claim 55 further comprising:

creating a second via at a second location where interconnect lines from at least three layers intersect.

59. A method of simulating Euclidean wiring, said method comprising:

determining a preferred wiring angle for a metal layer;

determining a ratio of an interconnect line length along a first direction to a diagonal interconnect line length along a second direction that is approximately 45 degrees from said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle.

60. The method of claim 59 wherein said first direction is horizontal and said second direction is 45 degrees.

61. The method of according to claim 59 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of an interconnect line length along said first direction and a diagonal interconnect line length along said second direction.

62. A method of simulating Euclidean wiring, said method comprising:

determining a preferred wiring angle for a metal layer;

determining a ratio of a first interconnect line length along a first direction to a second interconnect line length along a second direction that is approximately 90 degrees from said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle.

63. The method of claim 62 wherein said first direction is horizontal and said second direction is vertical.

64. The method of according to claim 62 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of an interconnect line length along said first direction and an orthogonal interconnect line length along said second direction.

65. An integrated circuit layout, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

a third interconnect line layer, said third interconnect line layer having a first arbitrary diagonal preferred direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said first subsegment.

66. The integrated circuit layout as claimed in claim 65, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

67. The integrated circuit layout as claimed in claim 66 wherein said first diagonal preferred direction is approximately forty-five degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative forty-five degrees relative to said preferred horizontal direction.

68. The integrated circuit layout as claimed in claim 66, said integrated circuit layout further comprising:

a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction orthogonal to said first diagonal preferred direction wherein interconnect lines on said fifth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

69. A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said first subsegment

70. The method of laying out said integrated circuit layout as claimed in claim 69, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

71. The method of laying out said integrated circuit layout as claimed in claim 69, said method wherein said first diagonal preferred direction is approximately

forty-five degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative forty-five degrees relative to said preferred horizontal direction.